

2012 International Symposium on Extreme Ultraviolet Lithography

Brussels, Belgium
30 September – 4 October 2012



EUVL mask blank requirements toward high volume manufacturing

Hwan-Seok Seo,* Sungmin Huh, Suyoung Lee, Tae-Geun Kim, Seong-Sue Kim, and Chan-Uk Jeon

SAMSUNG Electronics

Contents

☐ Introduction

☐ Blank defect requirements

- ✓ Defectivity, Printability, Inspection, Defect mitigation, Specification for defect free mask

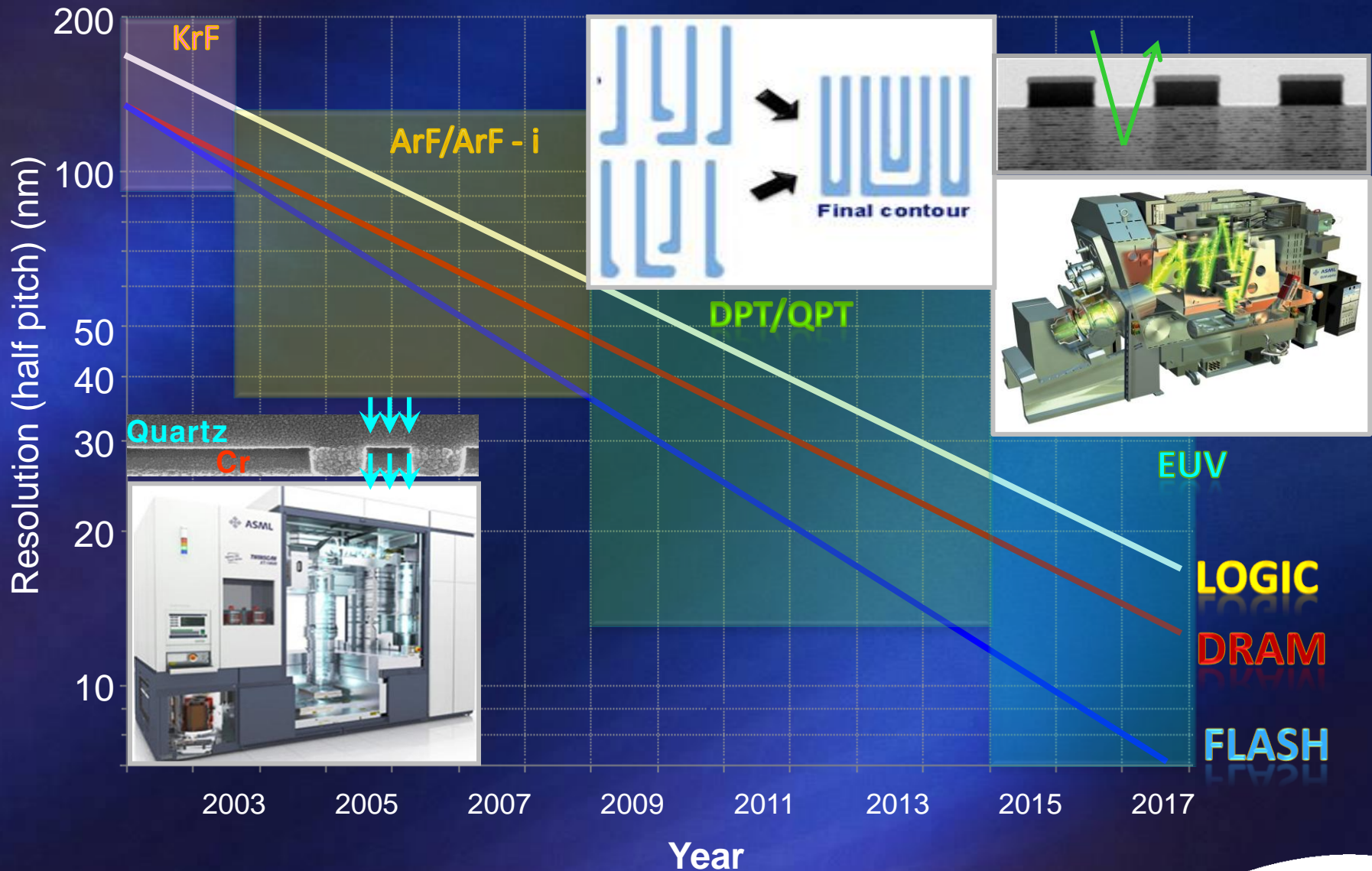
☐ Blank quality requirements

- ✓ Contamination & Lifetime, Actinic characteristics, Roughness & Non-flatness, Absorber stack

☐ Summary & Conclusions

Evolution of litho technology

H. Cho, 2011 EUVL Symposium in Miami



EUV focus area in 2007-2011

2007 / 22hp	2008 / 22hp	2009 / 22hp	2010 / 22hp	2011 / 22hp
1. Reliable high power source & collector module	1. Long-term source operation with 100 W at IF and 5MJ/day	1. Mask yield & defect inspection/review infrastructure	1. Mask yield & defect inspection/review infrastructure	1. Long-term reliable source operation with 200 W at IF*
2. Resist resolution, sensitivity & LER met simultaneously	2. Defect free masks through lifecycle & inspection/review infrastructure	2. Long-term reliable source operation with 200 W at IF	1. Long-term reliable source operation with 200 W at IF	2. Mask yield & defect inspection/review infrastructure
3. Availability of defect free mask	3. Resist resolution, sensitivity & LER met simultaneously	3. Resist resolution, sensitivity & LER met simultaneously	2. Resist resolution, sensitivity & LER met simultaneously	3. Resist resolution, sensitivity & LER met simultaneously
4. Reticle protection during storage, handling and use	• Reticle protection during storage, handling and use	• EUVL manufacturing integration	• EUVL manufacturing integration	• EUVL manufacturing integration
5. Projection and illuminator optics quality & lifetime	• Projection / illuminator optics and mask lifetime			

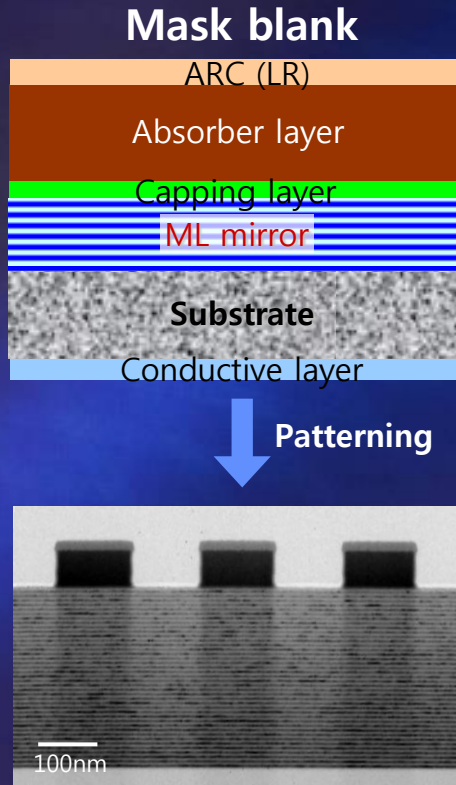
Ref) International EUVL Symposium Program Steering Committee, 2007 - 2011

- ❑ Delay in source development is the top show stopper which retards successful implementation of EUVL unanimously, and then **preparation of defect-free mask** is the next one.

Mask related issues

Category	Issues to check
Mask blank	Defects (substrate, ML)/inspection/printability, EUVR (CW/ R_{peak} /bandwidth, mean value & uniformity), Non-flatness, Surface & interface roughness, Absorber thickness & uniformity, FM process on ML or substrate
Mask process	CD control, LER/RSR, Defect mitigation (compensation) & repair, Pattern mask inspection, Cleaning durability
Wafer exposure	OPC (flare, shadow effect), Black border effect, Mask induced overlay/LWR/LCDU, Contamination from scanner (front/back)
Lifetime	Carbon contamination, Frequency of cleaning, Limit of max exposure numbers, Storage
Handling	Dual pod, pellicle(?)
Infra & Tools	Absence of actinic defect inspection & review tool

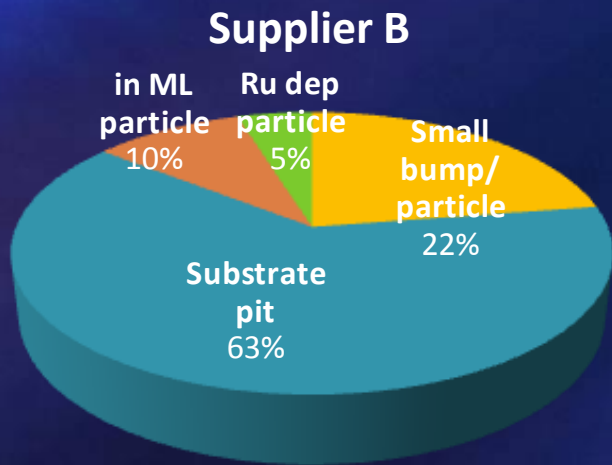
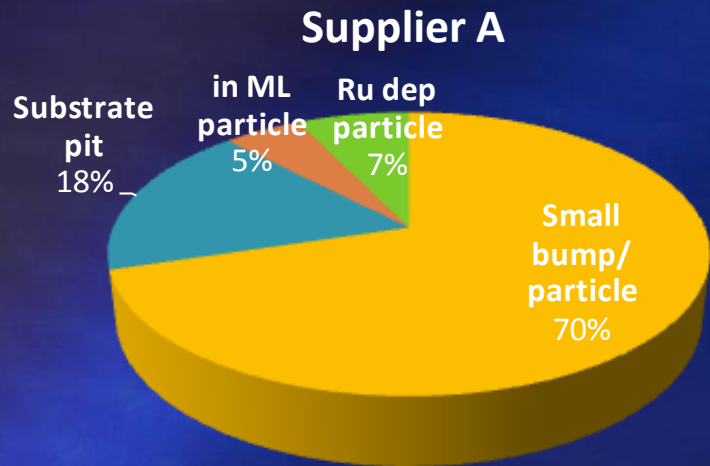
Mask blank for EUV lithography



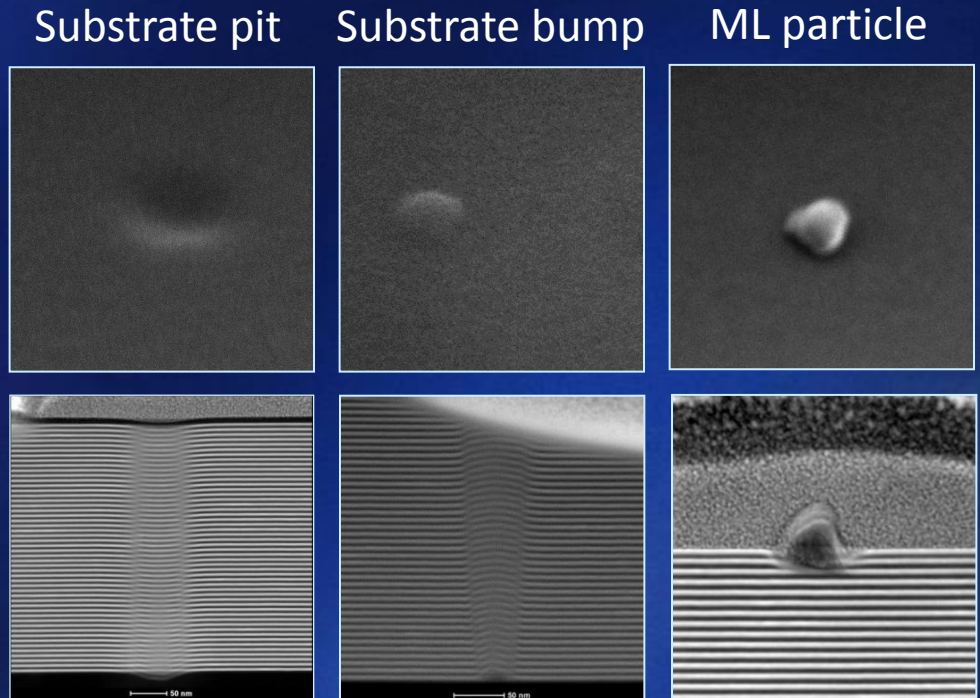
Layer	Materials	Main Role	Current Focus
ARC (LR)	TaON, TaO, TaBO, etc.	Inspection sensitivity @193nm	Thickness optimization for litho performances & mask process compatibility
Absorber	TaN, TaBN, TaB, etc.	Litho performances @EUV (contrast, NILS, LWR, CDU...)	
Capping	Ru, Ru alloy	Protecting ML (etch, CLN, repair, handling, exposure)	Damage (from Etch, CLN, Repair)
ML mirror	Mo/Si 40-50 pairs	Reflection mirror @EUV	Defect, Stability, EUVR (CW, R_{peak} , BW)
Substrate	LTEM 6025 (ULE [®] , AZ [®] ...)	Supporting mask structure, Low thermal expansion	Defect (polish, CLN), Non-flatness
Backside	CrN, etc.	Electrostatic chucking @EUV scanner	E-chucking damage, Bowing control

- ❑ Material selection as well as defect control is essential for EUVL blanks to enhance mask performances.
- ❑ Blank structure should be evolved with decreasing design rule.

Defects in commercial blanks



H. Seo, 2011 EUVL Symposium in Miami

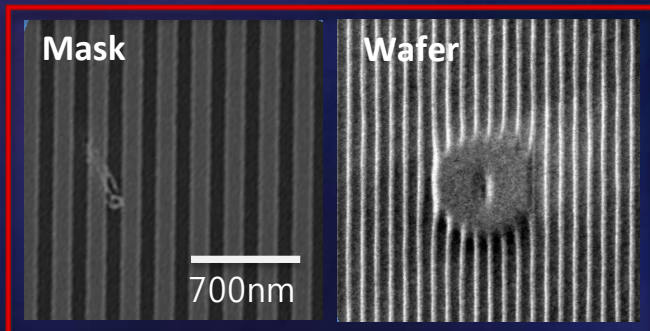
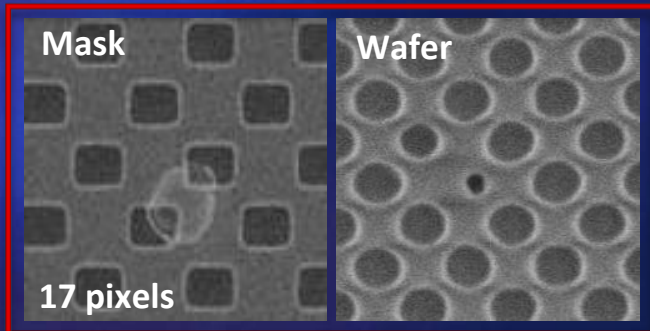
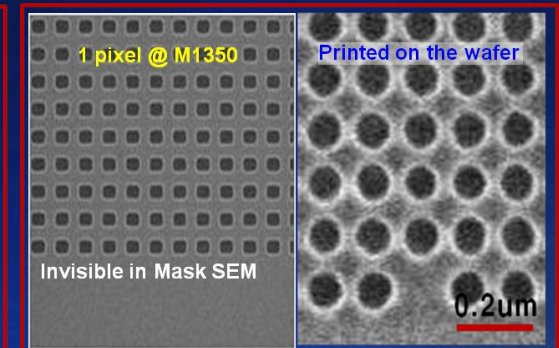
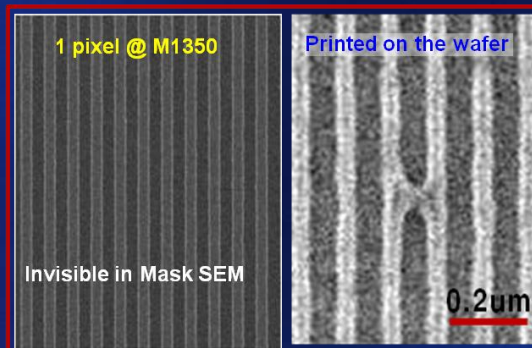
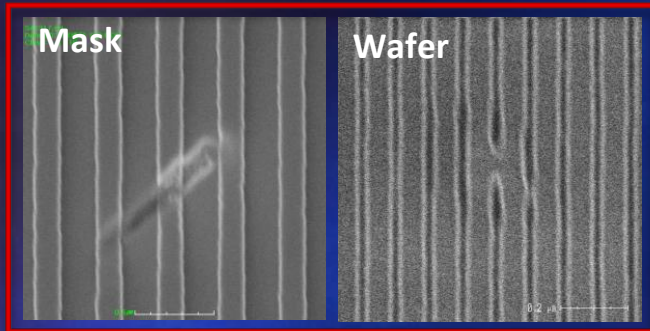


Ref) M. Goldstein (SEMATECH), 2011 EUVL Symposium
Jenah Harris-Jones (SEMATECH), SPIE 2012

❑ Major defect sources in ML blanks

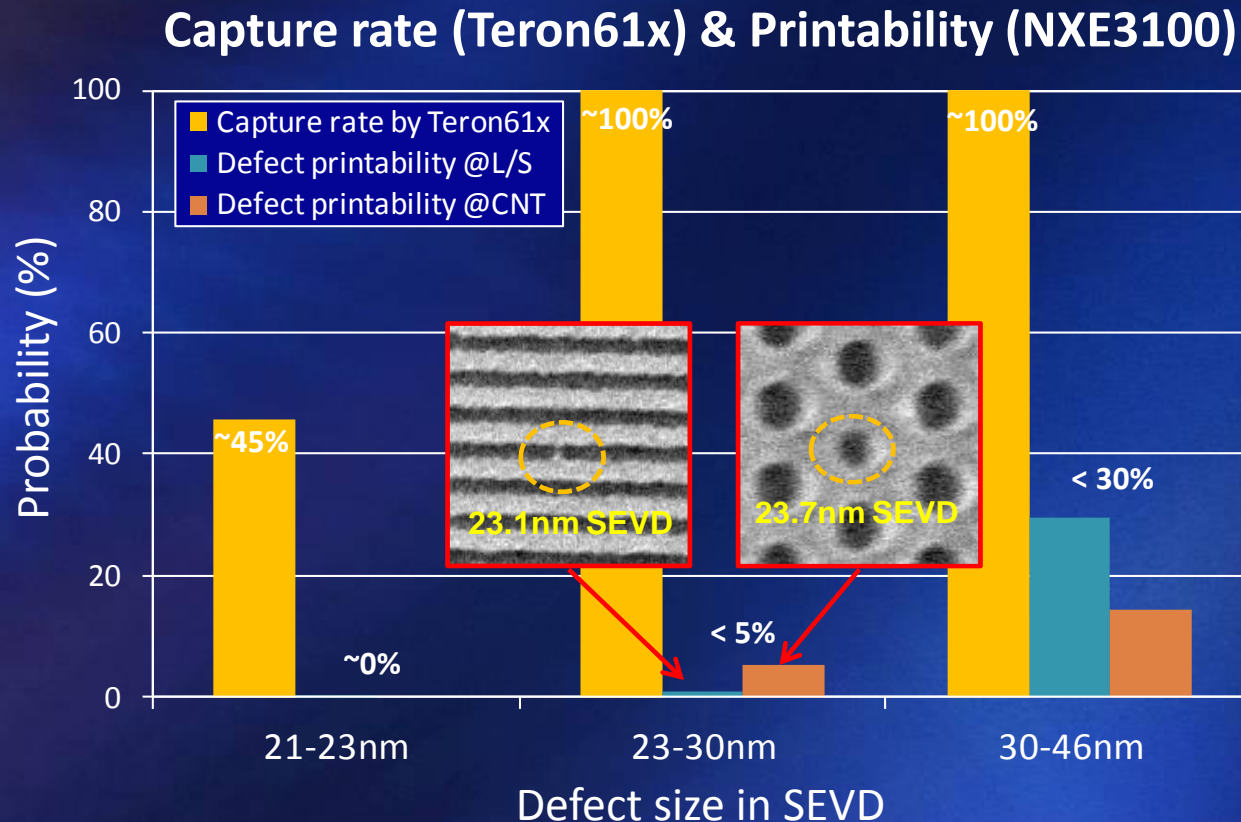
- ✓ Substrate polishing & cleaning (small)
- ✓ Ru/ML deposition (large)
- ✓ Handling (very large)

Printed phase defects on the wafer



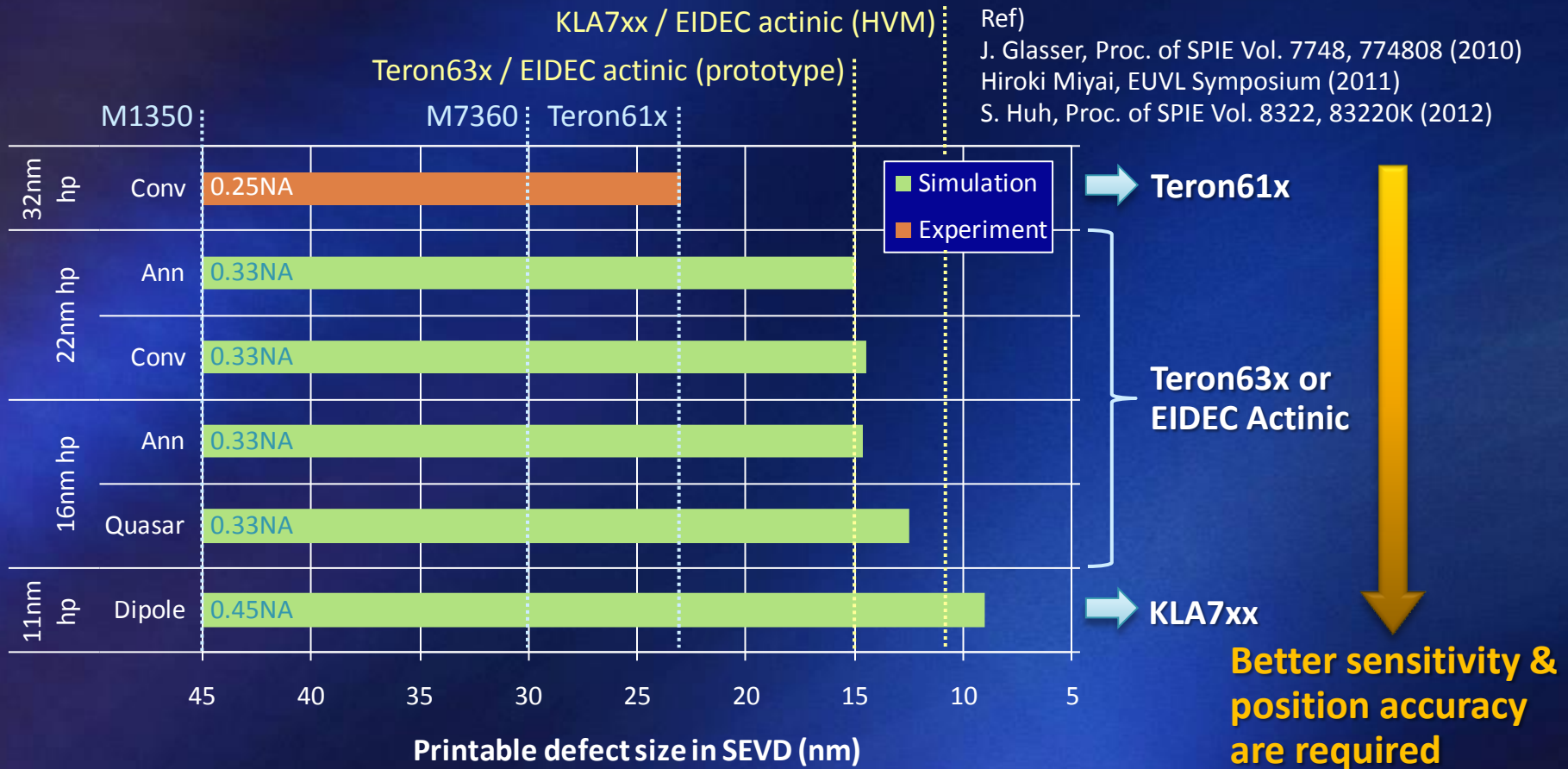
- ☐ Invisible defects by mask SEM could be printed on the wafer.
- ☐ Size of defective area on the wafer does not depend on defect size on the mask surface and pixels in BI tool.
- ☐ Actinic defect inspection and review tool are required to predict reliable defect printability.

Blank defect printability @32nm hp



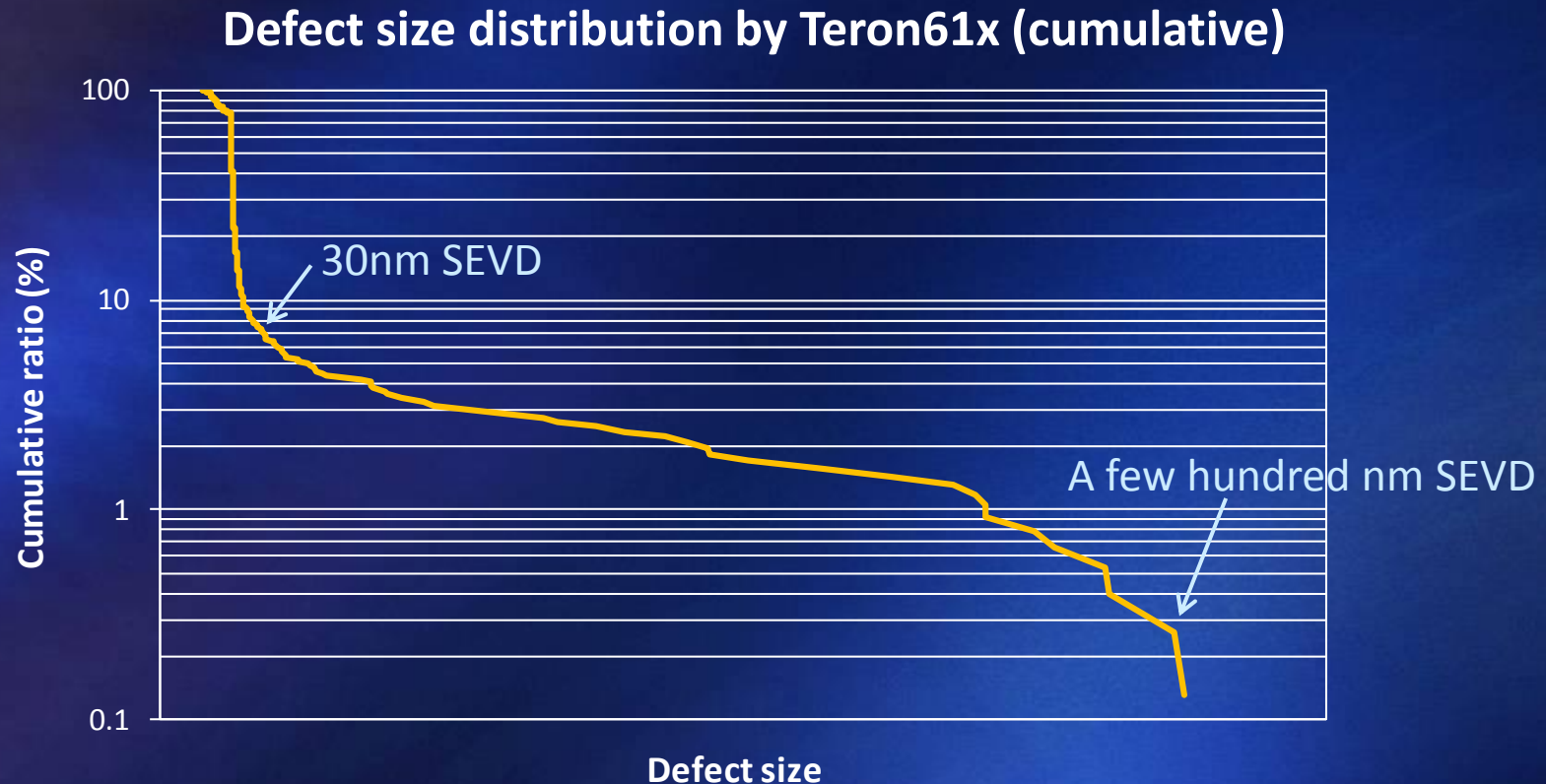
- ~23nm in SEVD is minimum printable defect size @32nm hp node.
- Teron61x could capture most of defects with >23nm SEVD in size.

Printability estimation for next generation



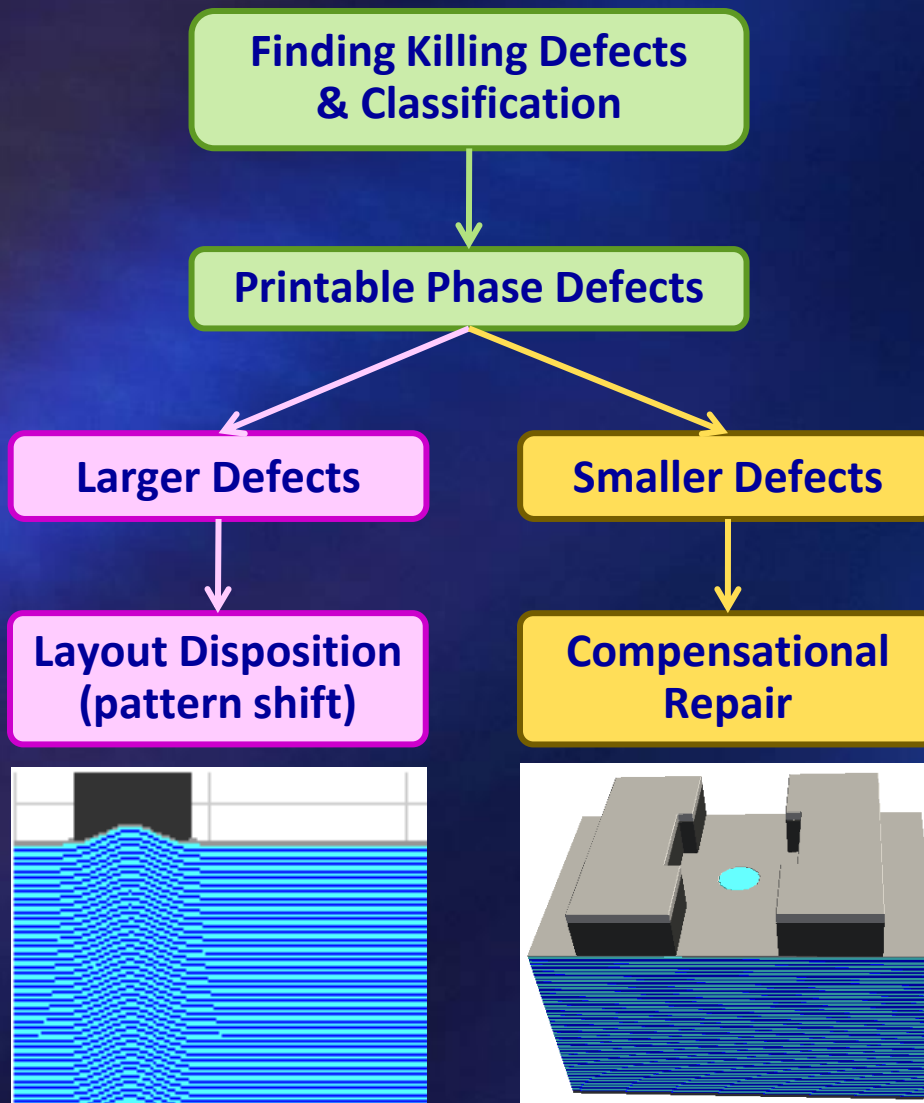
- ❑ Real printability results using EUV HVM tool (0.33NA) should be updated to evaluate limit of each BI tool.
- ❑ For HVM of 22nm hp node, a new BI tool should be applied.

Defect size distribution in current blank



- ❑ Defect level dramatically increases below ~30nm in SEVD.
- ❑ Lots of defects with <23nm would be printable at 22nm hp node.
- ❑ For reliable inspection of defects with <23nm SEVD, advanced BI tools are required.

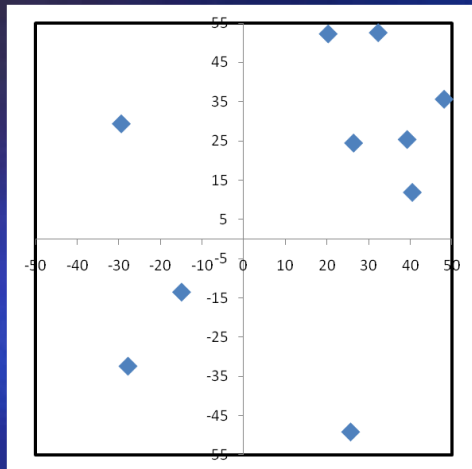
Additional defect mitigation



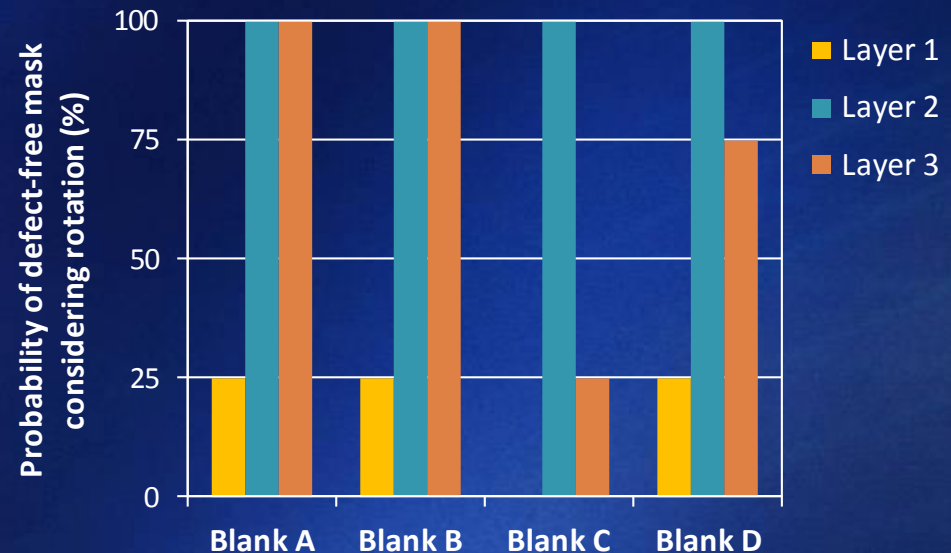
- ❑ To improve mask yield for HVM, additional defect mitigation process should be considered.
- ❑ Layout disposition and compensational repair are two main defect mitigation strategies.
- ❑ Prerequisites for defect mitigation
 - ✓ Fiducial mark on the blank
 - ✓ Defect review infra

Possibility of zero-printable defect mask

A blank with 10 defects @M1350



Defect mitigation based on M1350 data



S. Huh, Proc. of SPIE Vol. 8322, 83220K (2012)

- ❑ ~10 blank defects could be mitigated by blank rotation & pattern shift during e-beam writing for typical DRAM.
- ❑ Supply of blanks with ≤ 10 printable defects is essential to attain defect-free mask.

Key factors in mitigation for defect-free mask

❑ Total defect counts in blanks

- ✓ Normally less defects enhance the possibility of defect-free mask but their locations are also important.

❑ Defect size distribution in blanks (no large defects)

- ✓ Existence of large (killer) defects dramatically reduces the opportunity of defect-free mask. Effort to reduce large defects should be accelerated by blank suppliers.

❑ Defect coordinates & size accuracy, and e-beam alignment

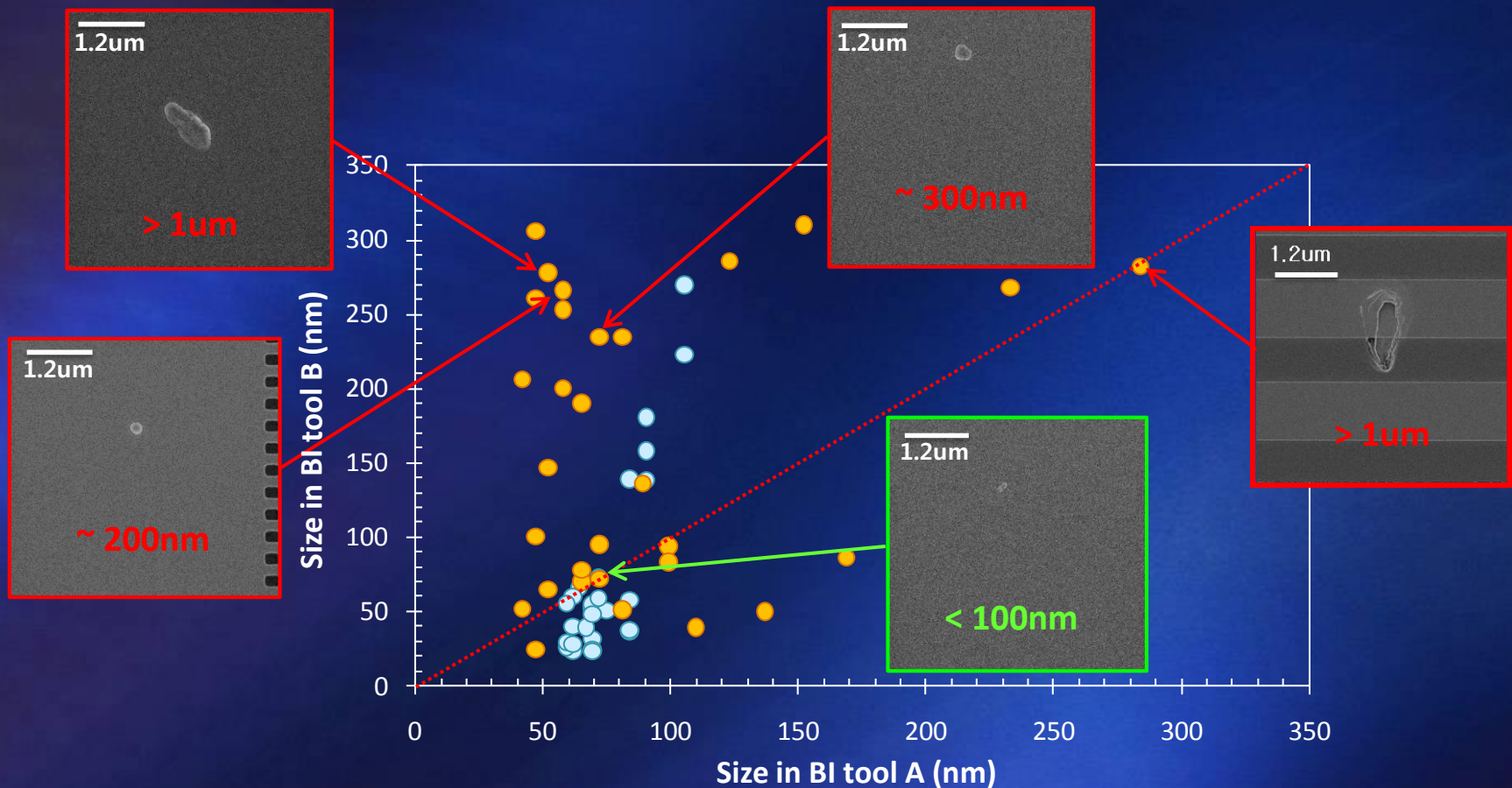
- ✓ Metrology tools must meet the specification.

❑ Reliable & defect-free FM (fiducial mark) process

- ✓ Blank suppliers should install the process and related infra.

❑ Defect verification infra (AIMS™, Wafer printing, etc.)

Issues in blank inspection: size uncertainty



- ❑ Big differences in size exist among BI tool A, B, and SEM measurements.
- ❑ Size accuracy should be guaranteed in BI tools for effective defect mitigation.

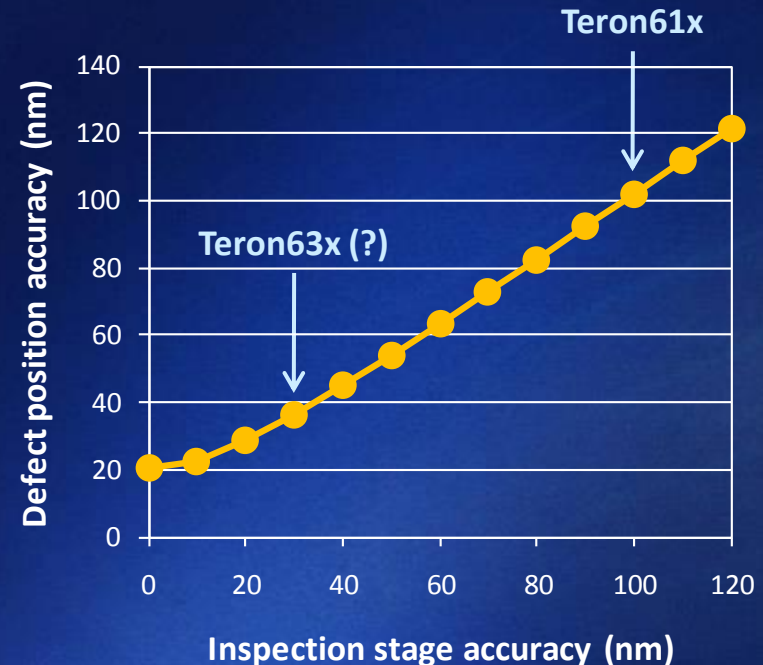
Issues in blank inspection: position accuracy

Defect position accuracy for defect mitigation is given by

$$\sigma^2(A) = \sigma^2(B) + \sigma^2(C) + \sigma^2(D)$$

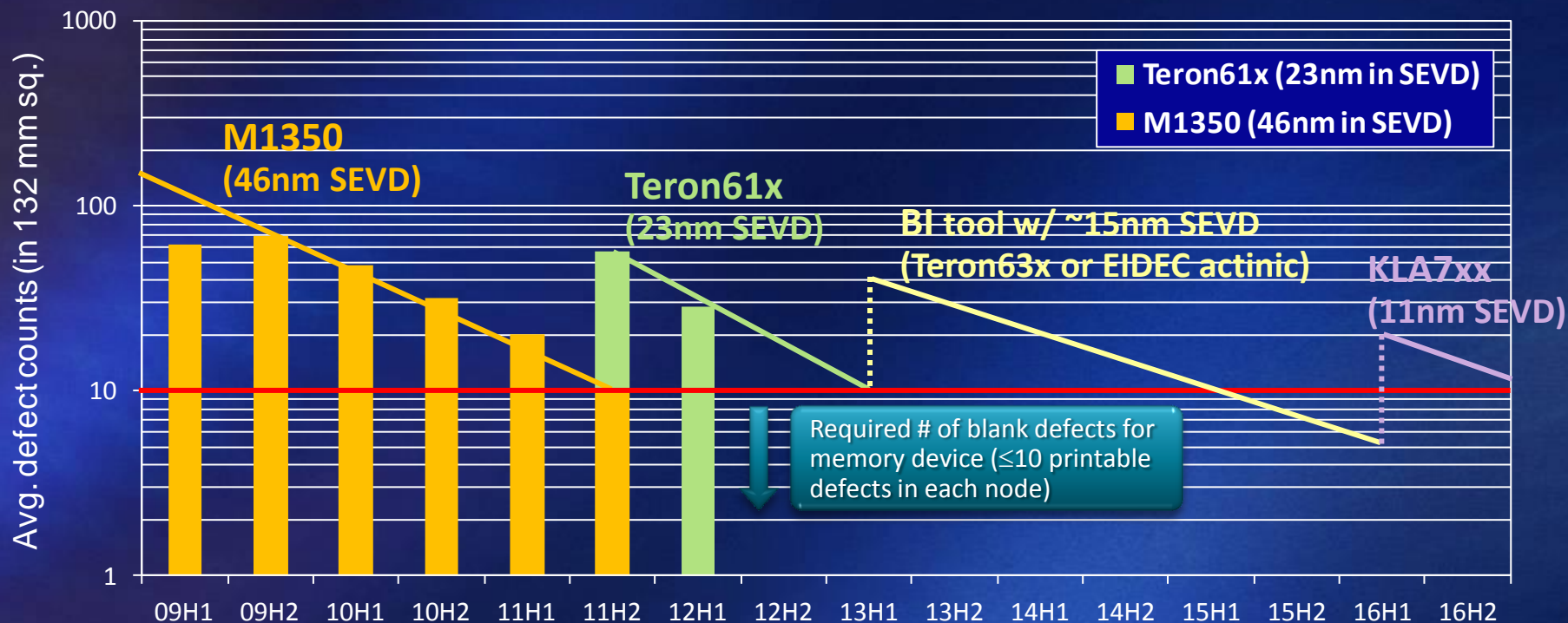
Where,

- A: Uncertainty of defect position under absorber
- B: Inspection stage accuracy (depending on BI tool)
- C: e-beam alignment accuracy to FM (~20nm)
- D: e-beam stage accuracy (~3.8nm)



- ❑ Stage accuracy in current BI tool is much worse than e-beam tool.
- ❑ Stage accuracy with < 30nm is required in BI tools for reliable defect mitigation.

Roadmap for blank defect reduction



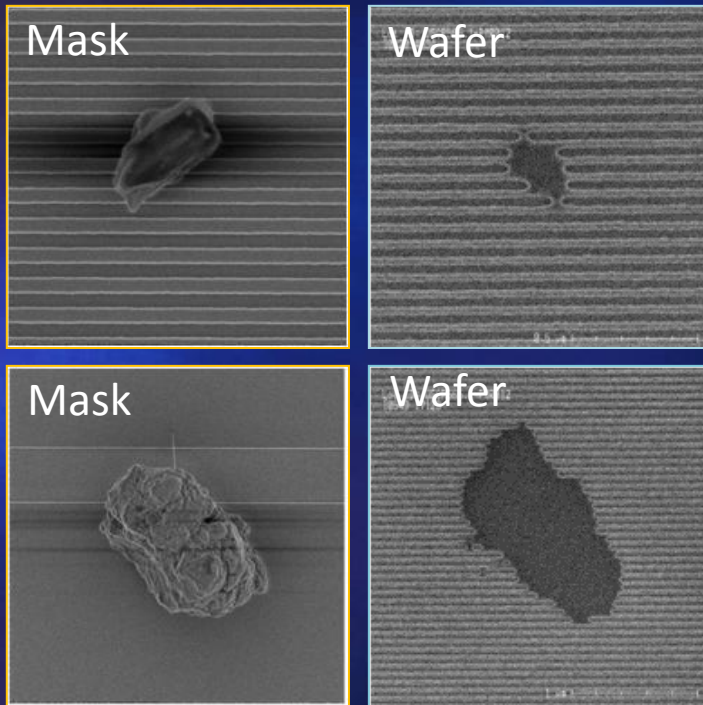
- Blank defect reduction has been accelerated by both suppliers. At the same time, yield of quality blank should be increased.
- ≤ 10 printable defects per plate in each node would be practical spec for HVM of memory device.
- Corresponding BI tool should also be commercialized on time.

Summary-1: blank defect requirements

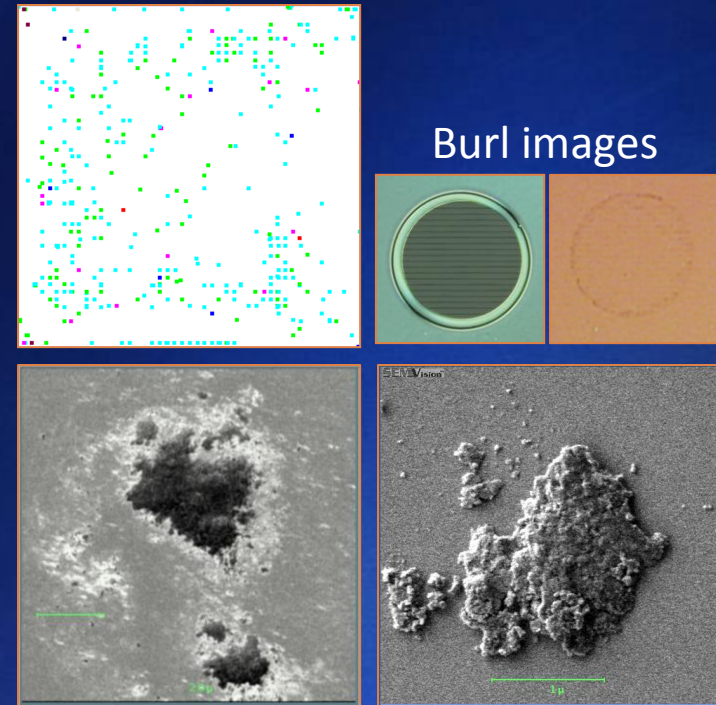
- ❑ ~23nm in SEVD is minimum printable defect size for 32nm hp node but smaller defects should be controlled for HVM of 22nm hp node and beyond.
- ❑ Recently, defect reduction has been accelerated by suppliers and 1-digit numbers @60nm (M1350) were attained. More reduction and yield increase are required to produce adequate quality blanks for HVM.
- ❑ ML defect mitigation and compensational repair are two main strategies to produce defect-free masks. Accuracy in defect size & position, reliable FM process, and defect verification method should also be prepared.
- ❑ For memory devices, ≤ 10 printable blank defects might be allowed for HVM. BI tools and blanks to meet the requirements need to be prepared on time.

Reticle contamination from EUV scanner

✓ Front side contamination



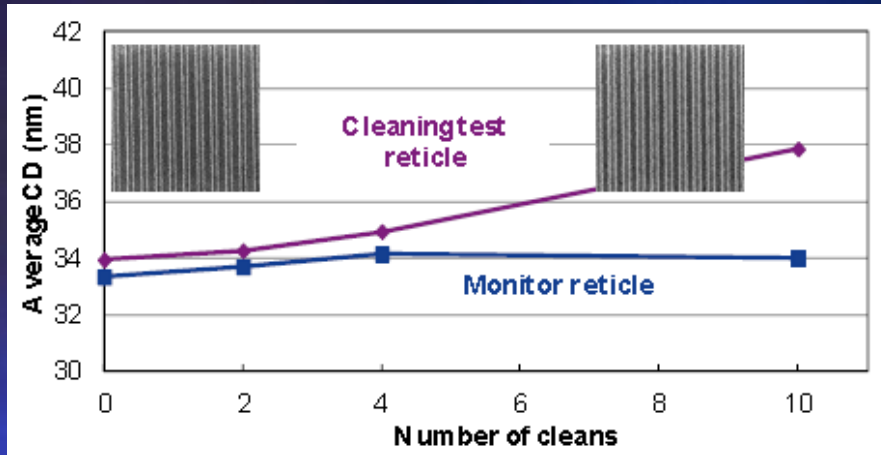
✓ Backside contamination



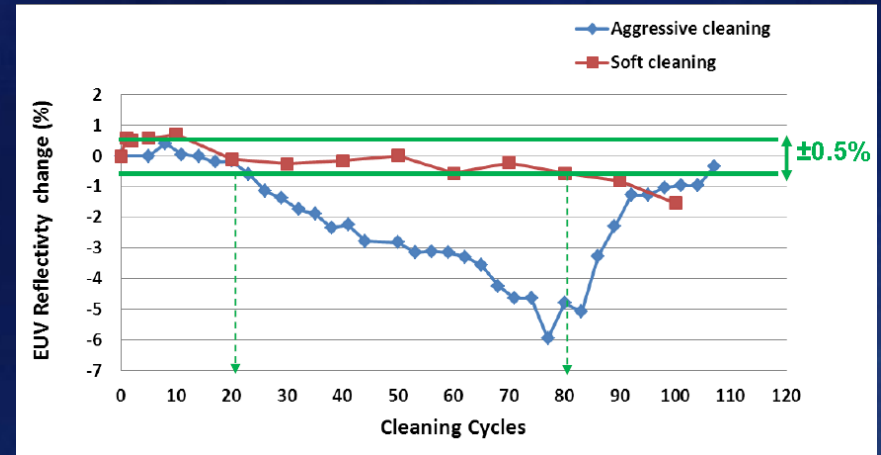
Courtesy of C. Jeong

- ❑ Reticle contamination from scanner is one of the big concerns.
- ❑ Maintenance of system cleanliness as well as development of related infra (e.g. pod, pellicle?) and mask process (e.g. cleaning) is required.

Lifetime of EUV reticle



Ref) R. Jonckheere, Proc. of SPIE Vol. 8352, 83520U



Ref) A. Rastegar, 2011 EUVL Symposium in Miami

- ❑ Due to absence of pellicle & high power of source, MTBC (mean time between cleanings) of EUV reticle is much shorter than optical reticle.
- ❑ Lifetime of EUV reticle considering max frequency & cycle of EUV exposure and cleaning should be determined.
- ❑ Improvement of blank material and cleaning process is also required to enhance durability of mask (i.e. less CD & reflectivity changes and Ru damage).

Actinic wavelength characteristics

- ❑ Non-uniformity of actinic reflectivity in blank results in CD error on the wafer.
- ❑ Especially, deviation of CW from target value results in global CD error. To make min CD error due to mask CW, we need to consider...
 - ✓ Max broadband mask reflectivity to make min dose & CD variation (Optimal CW = $13.52 \pm 0.01 \text{ nm}$ for NXE3100)
 - ✓ Min apodization to make small mask induced telecentricity & pattern displacement (Optimal CW = $13.54 \pm 0.01 \text{ nm}$ for NXE3100)
 - ✓ **Mean CW spec for NXE3100 = $13.53 \pm 0.014 \text{ nm}$**

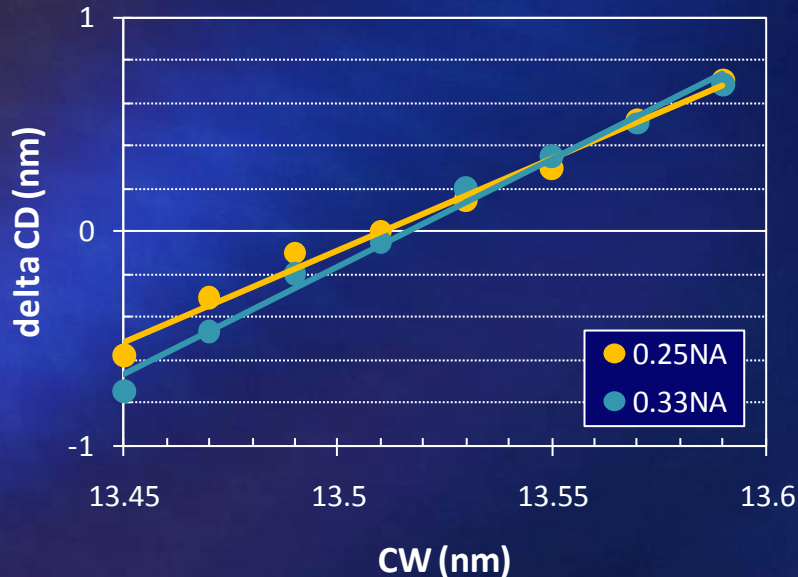
Ref) N. Davydova, Proc. of SPIE Vol. 8166, 816624-6 (ASML)

- ❑ However, mean CW variation of current commercial blank is 2-3x larger than ASML's spec.

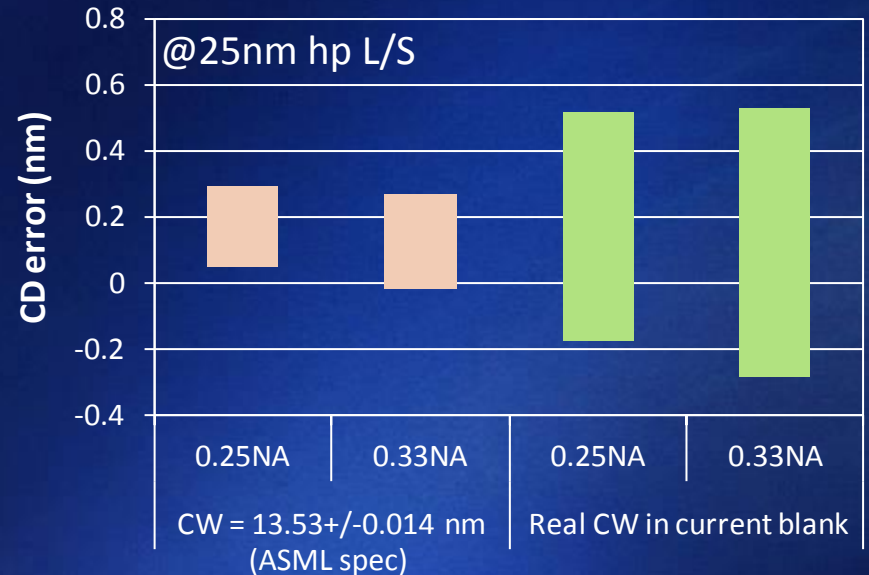
Center wavelength (CW) optimization

□ Preliminary simulation results

CD error due to 0.04nm CW non-uniformity



CD error as a function of NA & CW range



Remarks: Broadband spectrum & variations in illumination are not applied in the simulation

- Mean CW variation results in CD error on the wafer pattern.
- Current mean CW range & non-uniformity in blanks give rise to -0.3 to 0.5nm (1x) CD errors on the wafer.

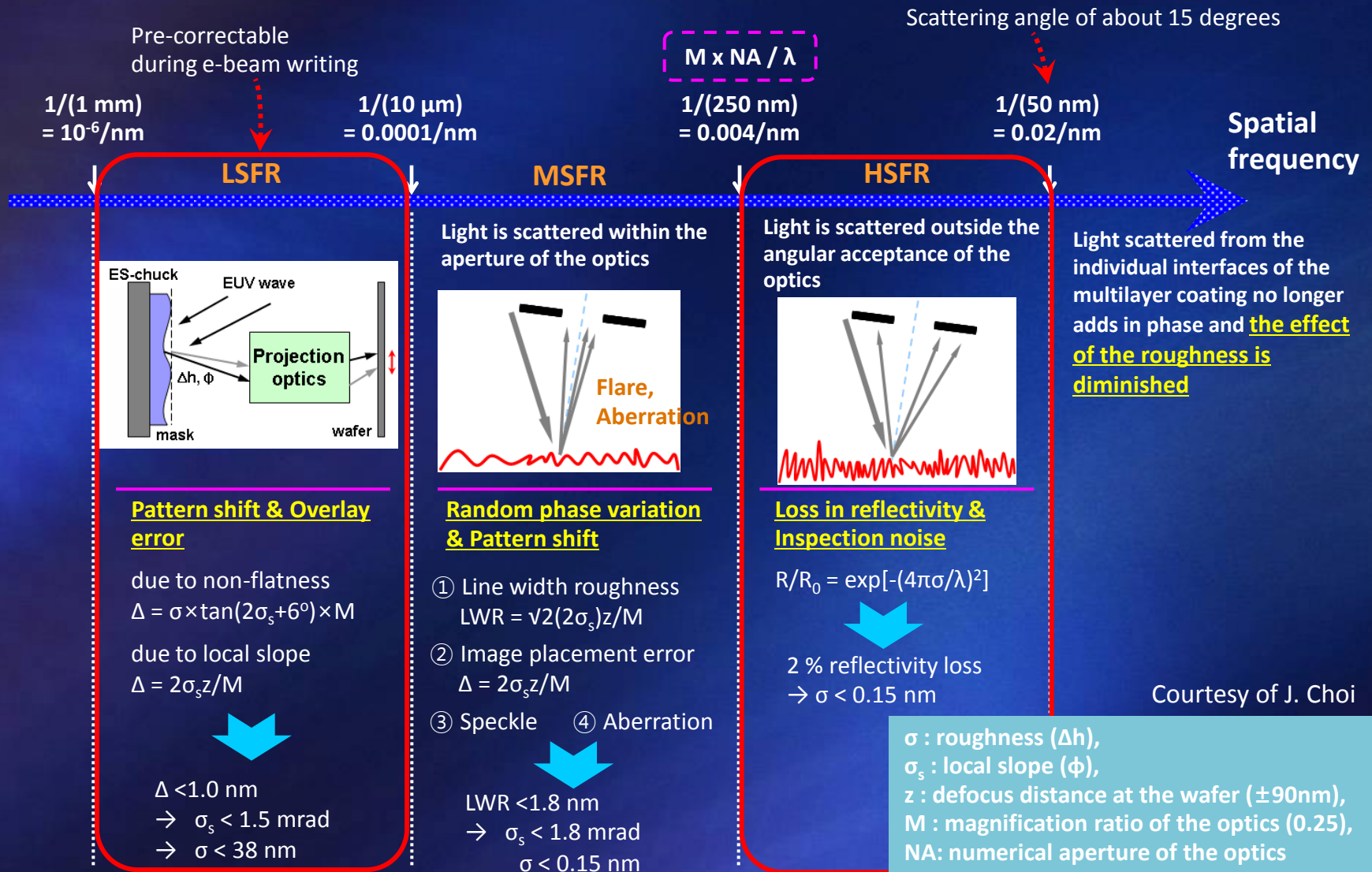
Spec for actinic wavelength characteristics

ASML's spec for the actinic wavelength of ML for NXE3100

Parameter	Specification	Status
Mean center wavelength (CW)	13.53 nm	☹️
Mean center wavelength shift	$\leq 0.1 \%$ (13.516 - 13.543 nm)	☹️
Mean FWHM of reflectivity vs. wavelength	≥ 0.5 nm	😊
Max range of bandwidth @FWHM	0.005 nm	😊
Max range of center wavelength	0.04 nm	😐
Mean peak reflectivity	$\geq 67 \%$	☹️
Max range of peak reflectivity	0.3 %	😐

- ❑ CW, peak reflectivity, bandwidth at actinic wavelength and their mean values & uniformity should be tightly controlled.
- ❑ Spec for actinic characteristics depends on optics (illumination cone & diffraction angle) of EUV scanner. Thus, revised spec for NXE3300 should be prepared and applied for EUV ML blank.

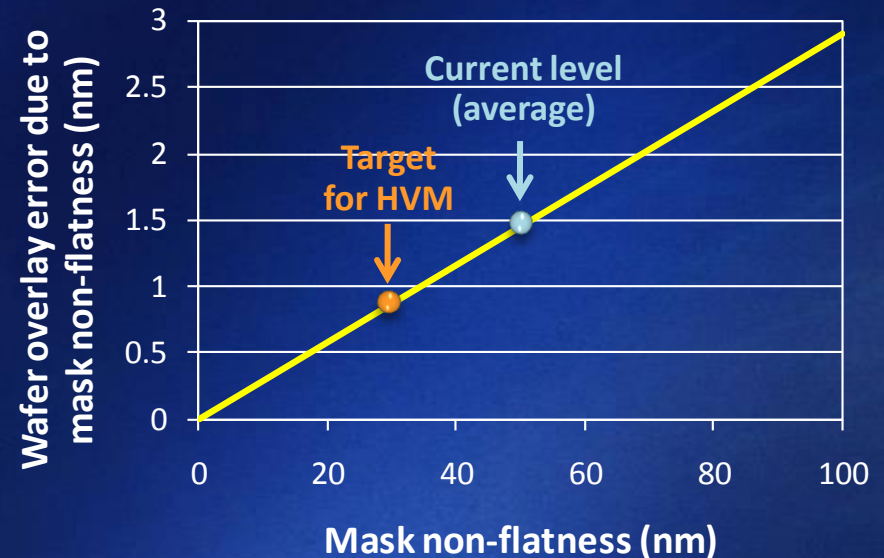
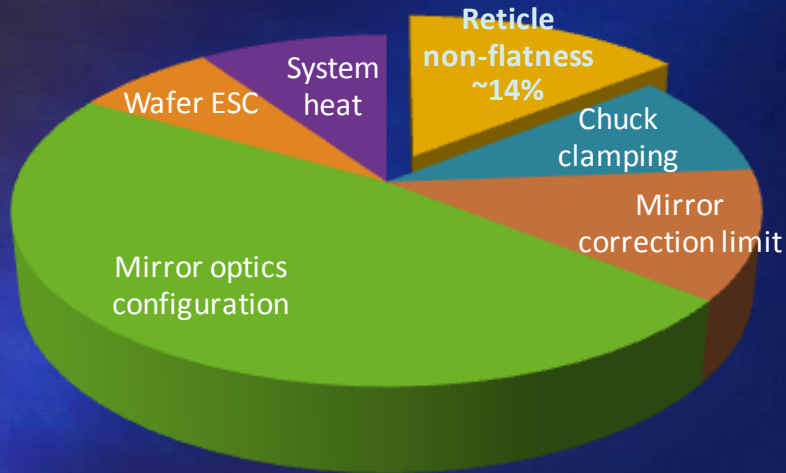
Roughness of EUV mask



Reference: E. Gullikson, "Proposed specification of EUVL mask substrate roughness," 2nd International EUVL Symposium (2003).
 SEMI P37-1102, SEMI Standard Specification for Extreme Ultraviolet Lithography Mask Substrates (2002).
 S. Yoshitake, et. al, EUV Mask Flatness & Carrier/Loadport Workshop (2006)

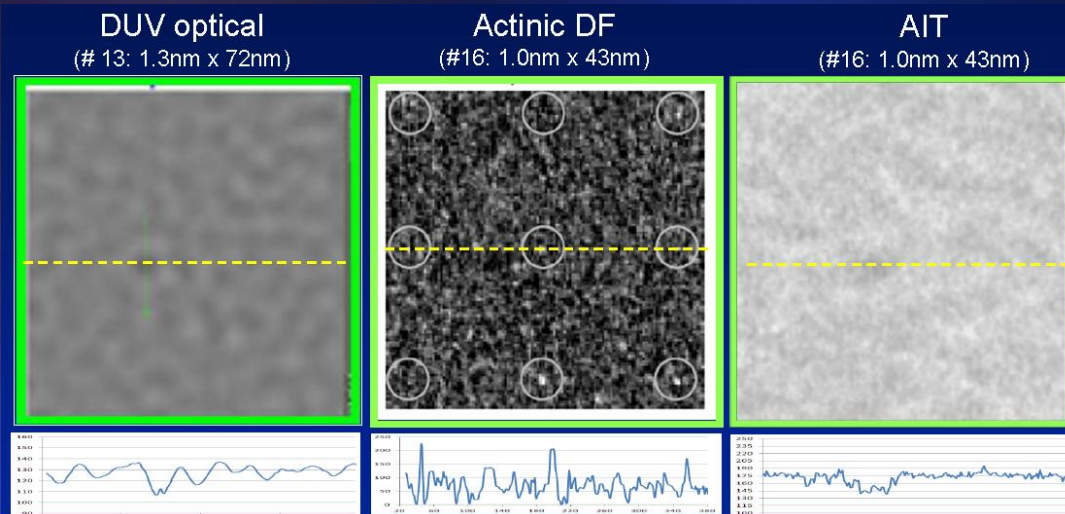
Blank non-flatness effects on wafer overlay

Current overlay budget for EUVL

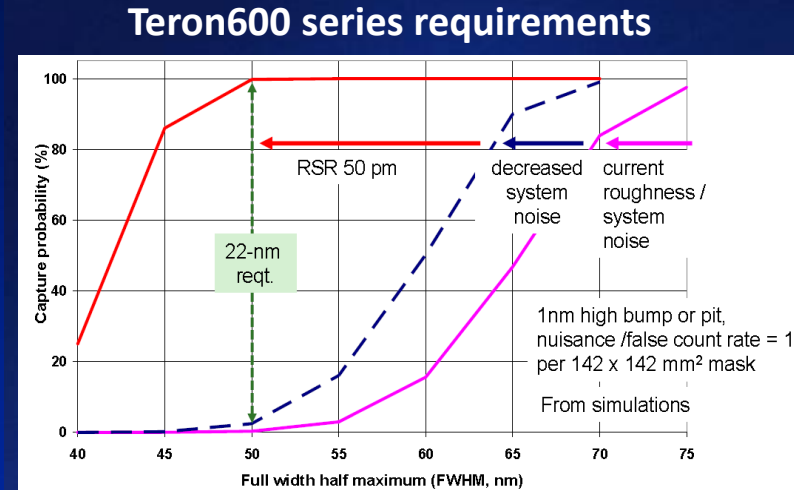


- Portion of reticle non-flatness term is regarded as ~14% of total wafer overlay budget.
- Continuous improvement of non-flatness as well as development of flatness compensation technique is essential.

ML roughness effects on blank inspection



Ref) T. Liang, 2011 EUVL Symposium in Miami



Ref) G. Inderhees, PMJ (2011)

- ❑ ML roughness results in background noise during blank inspection.
- ❑ Next generation BI tool should discriminate between printable defects and roughness noise.
- ❑ High frequency surface roughness should be reduced and roughness spec for reliable BI should be established for HVM of 22nm node.

Absorber stack requirements

Item	Requirements
Materials	Currently, Ta-based alloy is usual. Compositions could be determined by lithography & mask process.
Defects	Should be manageable (size & numbers) considering mask repair capability.
Thickness (AR + Abs)	H-V bias and black border effect could be calibrated by OPC & mask process (e.g. ML etch @border). Optimum thickness should be determined considering lithography performance & mask process compatibility (inspection, etch,...).
Thickness variation*	± 0.5 % of thickness
Reflectivity @wavelength*	<ul style="list-style-type: none"> • Actinic R < 2 % @13.395-13.665nm • DUV R \leq 25 % @130-320 nm (need to check PMI sensitivity) • Visible wavelength contrast to ML \geq 14 % @470nm • IR R \leq 80 % @780-860nm, 50-80 % @860-920nm, \leq 80 % @920-1000nm, \leq 90 % @1000-2000nm

* Spec for NXE3100 from ASML

Summary-2: blank quality requirements

- ❑ Due to absence of pellicle & high source power, contamination from scanner & handling is much severe in EUV mask. Lifetime of EUV reticle considering max frequency of EUV exposure and cleaning should be determined.
- ❑ To minimize CD error on the wafer, CW, R_{peak} , & bandwidth of ML at actinic wavelength must be tightly controlled. Revised spec for HVM tool should also be prepared and applied for ML blank.
- ❑ Non-flatness & roughness in blank increase wafer overlay error and noise level in BI tools, respectively. They should be reduced below target values for HVM.
- ❑ Spec for absorber stack needs to be determined considering lithography performance and mask process compatibility.

Conclusions

- ❑ EUVL mask and blank requirements for HVM are discussed.
- ❑ Defect reduction and quality improvement of EUVL blank have been progressed step by step in the past decade. For HVM, however, we need breakthrough on the on-time development of related technologies & infrastructures as well as blank itself.
- ❑ From now on, we need to determine the specifications for HVM and focus on the attainments.

Thank you for attention!